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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/835,170	04/13/2001	Spencer Gold	P5213/SMQ-041	4882

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EXAMINER	
CHAUDRY, MUJTABA M	
ART UNIT	**PAPER NUMBER**
2133	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/835,170	GOLD, SPENCER	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 24-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 24-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicants' response was received December 12, 2006.

- Claims 1-6 and 24-31 are rejected.

Application pending.

Response to Amendment

Applicant's arguments/amendments with respect to claims 1-6 and 24-31 filed December 12, 2006 have been received. All arguments have been fully considered but are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Applicant contends, "...Nakamura (prior art of record) does not teach or suggest a conversion circuit to convert physical address in the memory array to a logical address in the memory array to **allow said test vector to be written to said logical address of the memory**." The Examiner respectfully disagrees. The Examiner would like to point out that Nakamura teaches (i.e., col. 3, lines 43-56) to determine the physical addresses of the DRAM and then (i.e., col. 3, lines 57-65) allows the BIST circuitry to generate test patterns. It is clear that the bitmap converter is used to allow the test pattern to be written to appropriate logical addresses of the memory. It is important to note that the conversion is necessary to allow the test vector be written to the logical address of the memory. Emphasis added.

The Examiner disagrees with the Applicant and maintains rejections with respect to claims 1-6 and 24-31. All arguments have been considered. It is the Examiner's conclusion that claims 1-6 and 24-31, as presented, are not patentably distinct or non-obvious over the prior art of record. See office action:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

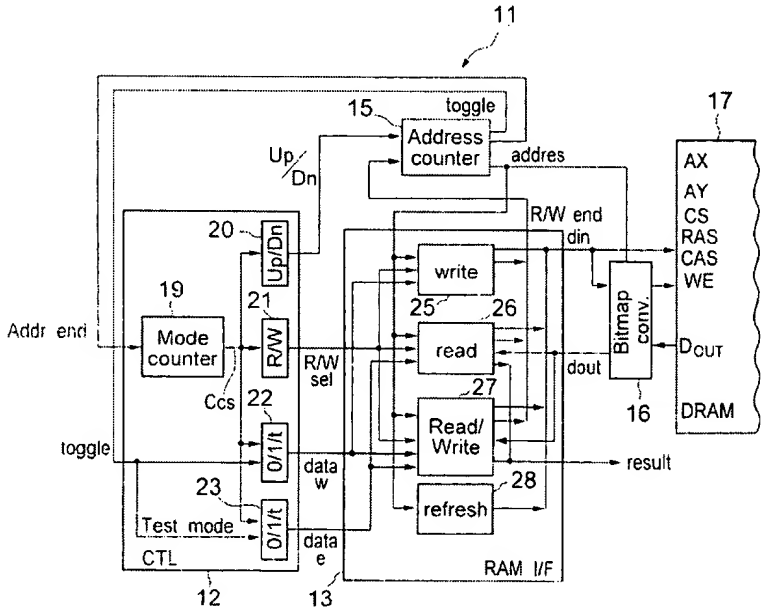
> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakamura (USPN 6523135).

As per claim 1, Nakamura teaches (Figure 1 and col. 3) a BIST circuit 11, a test mode controller 12, a RAM interface 13, an address counter 15 and a bitmap converter 16. The BIST circuit 11 is built in a DRAM 17 or in a system LSI including a DRAM 17 for testing the function of the DRAM 17. In the BIST circuit 11, the configurations for allowing the DRAM 17 to operate in a burst mode with a specified burst length, as well as in the CAS (column address strobe) latency, are determined by the user. The BIST circuit 11 consecutively generates a plurality of test patterns for testing the DRAM 17. The test mode controller 12 includes the mode counter 19, and also includes a first decoder 20 for generating an Up/Down control signal "Up/Dn", a second decoder 21 for generating a read/write selection signal "R/W sel", i.e., a read,

write or read/write signal for selecting a read mode, a write mode or a read/write mode, a third decoder 22 for generating write data "dataw", and a fourth decoder 23 for generating expected data "datae" for read data, all based on a count, or common control signal "Ccs", output by the mode counter 19. The Examiner would like to point out that Nakamura teaches (col. 3, lines 46—col. 4, lines 1-6) various test pattern generation techniques, wherein physical addresses are generated. Nakamura also teaches (Figure 1) the Bitmap converter 16 to enable writing to test data to the memory, by converting the physical address in the memory to a logical address. See Figure 1:

FIG. 1



As per claim 24, Nakamura teaches (Figure 1 and col. 3) a BIST circuit 11, a test mode controller 12, a RAM interface 13, an address counter 15 and a bitmap converter 16. The BIST circuit 11 is built in a DRAM 17 or in a system LSI including a DRAM 17 for testing the function of the DRAM 17. In the BIST circuit 11, the configurations for allowing the DRAM 17

to operate in a burst mode with a specified burst length, as well as in the CAS (column address strobe) latency, are determined by the user. The BIST circuit 11 consecutively generates a plurality of test patterns for testing the DRAM 17. The test mode controller 12 includes the mode counter 19, and also includes a first decoder 20 for generating an Up/Down control signal "Up/Dn", a second decoder 21 for generating a read/write selection signal "R/W sel", i.e., a read, write or read/write signal for selecting a read mode, a write mode or a read/write mode, a third decoder 22 for generating write data "dataw", and a fourth decoder 23 for generating expected data "datae" for read data, all based on a count, or common control signal "Ccs", output by the mode counter 19. The Examiner would like to point out that Nakamura teaches (col. 3, lines 46—col. 4, lines 1-6) various test pattern generation techniques, wherein physical addresses are generated. Nakamura also teaches (Figure 1) the Bitmap converter 16 to enable writing to test data to the memory, by converting the physical address in the memory to a logical address.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 2-6 and 25-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura (USPN 6523135).

As per claims 2-4, Nakamura substantially teaches, in view of above rejections, (Figure 1) a RAM interface 13, which is coupled to the conversion circuit 16. Nakamura teaches (col. 4, lines 37-35) the RAM interface 13 includes a write circuit 25, a read circuit 26, read/write circuit 27 and a refreshing circuit 28, and executes a sequence of read, write or read/write operation by generating data and control signals for the read, write or read/write operation. The refreshing circuit 28 is activated each time the address counter 15 delivers 100 addresses, for example, to refresh data in all the memory cells of the DRAM 17. The Examiner would like to point out that although Nakamura does not explicitly teach the RAM interface to include ROM or EEPROM, these memory types are well known in the art to be used for reading data at a rapid pace as is done in testing.

As per claims 5-6, Nakamura substantially teaches, in view of above rejection, (col. 3, lines 43-45) to test the memory based on a wide variety of test patterns that are generated by any combination of column bars, checker board, marching, shifted diagonal, butterfly, walking and galloping. These variations allow testing for spatial locality of faults as well as transitional faults.

As per claims 25-27, Nakamura substantially teaches, in view of above rejections, (Figure 1) a RAM interface 13, which is coupled to the conversion circuit 16. Nakamura teaches (col. 4, lines 37-35) the RAM interface 13 includes a write circuit 25, a read circuit 26, read/write circuit 27 and a refreshing circuit 28, and executes a sequence of read, write or read/write operation by generating data and control signals for the read, write or read/write operation. The refreshing circuit 28 is activated each time the address counter 15 delivers 100 addresses, for example, to refresh data in all the memory cells of the DRAM 17. The Examiner would like to point out that although Nakamura does not explicitly teach the RAM interface to

include ROM or EEPROM, these memory types are well known in the art to be used for reading data at a rapid pace as is done in testing.

As per claims 28-29, Nakamura substantially teaches, in view of above rejection, (col. 3, lines 43-45) to test the memory based on a wide variety of test patterns that are generated by any combination of column bars, checker board, marching, shifted diagonal, butterfly, walking and galloping. These variations allow testing for spatial locality of faults as well as transitional faults.

As per claims 30 and 31, Nakamura substantially teaches, in view of above rejection, (col. 3, lines 46-57) physical mapping of the DRAM and logical mapping of the DRAM (col. 3, lines 58-65).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.

Mujtaba Chaudry
Art Unit 2133
January 17, 2007

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
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